processor or a central processing unit (CPU) **2704**. The illustrated CPU **2704** includes an Arithmetic Logic Unit (ALU) for performing computations, a collection of registers for temporary storage of data and instructions, and a control unit for controlling operation for the system **2700**. In one embodiment, the CPU **2704** includes any one of the x86, Pentium™, Pentium II™, and Pentium Pro™ microprocessors as marketed by Intel™ Corporation, the K-6 microprocessor as marketed by AMD™, or the 6x86MX microprocessor as marketed by Cyrix™ Corp. Further examples include the Alpha™ processor as marketed by Digital Equipment Corporation™, the 680x0 processor as marketed by Motorola™; or the Power PC™ processor as marketed by IBM™. In addition, any of a variety of other processors, including those from Sun Microsystems, MIPS, IBM, Motorola, NEC, Cyrix, AMD, Nexgen and others may be used for implementing CPU **2704**. The CPU **2704** is not limited to microprocessor but may take on other forms such as microcontrollers, digital signal processors, reduced instruction set computers (RISC), application specific integrated circuits, and the like. Although shown with one CPU **2704**, computer system **2700** may alternatively include multiple processing units.

[**0275**] The CPU **2704** is coupled to a bus controller **2712** by way of a CPU bus. The bus controller **2712** includes a memory controller **2716** integrated therein, though the memory controller **2716** may be external to the bus controller **2712**. The memory controller **2716** provides an interface for access by the CPU **2704** or other devices to system memory **2724** via memory bus **2720**. In one embodiment, the system memory **2724** includes synchronous dynamic random access memory (SDRAM). System memory **2724** may optionally include any additional or alternative high speed memory device or memory circuitry. The bus controller **2712** is coupled to a system bus **2728** that may be a peripheral component interconnect (PCI) bus, Industry Standard Architecture (ISA) bus, etc. Coupled to the system bus **2728** are a graphics controller, a graphics engine or a video controller **2732**, a mass storage device **2752**, a communication interface device **2756**, one or more input/output (I/O) devices $\mathbf{2768}_1$- $\mathbf{2768}_N$, and an expansion bus controller **2772**. The video controller **2732** is coupled to a video memory **2736** (e.g., 8 Megabytes) and video BIOS **2740**, all of which may be integrated onto a single card or device, as designated by numeral **2744**. The video memory **2736** is used to contain display data for displaying information on the display screen **2748**, and the video BIOS **2740** includes code and video services for controlling the video controller **2732**. In another embodiment, the video controller **2732** is coupled to the CPU **2704** through an Advanced Graphics Port (AGP) bus.

[**0276**] The mass storage device **2752** includes (but is not limited to) a hard disk, floppy disk, CD-ROM, DVD-ROM, tape, high density floppy, high capacity removable media, low capacity removable media, solid state memory device, etc., and combinations thereof. The mass storage device **2752** may include any other mass storage medium. The communication interface device **2756** includes a network card, a modem interface, etc. for accessing network **2764** via communications link **2760**. The I/O devices $\mathbf{2768}_1$-$\mathbf{2768}_N$ include a keyboard, mouse, audio/sound card, printer, and the like. The I/O devices $\mathbf{2768}_1$-**2768**N may be disk drive, such as a compact disk drive, a digital disk drive, a tape drive, a zip drive, a jazz drive, a digital video disk (DVD) drive, a magneto-optical disk drive, a high density floppy drive, a high capacity removable media drive, a low capacity media device, and/or any combination thereof. The expansion bus controller **2772** is coupled to non-volatile memory **2775**, which includes system firmware **2776**. The system firmware **2776** includes system BIOS, which is for controlling, among other things, hardware devices in the computer system **2700**. The system firmware **2776** also includes ROM **2780** and flash (or EEPROM) **2784**. The expansion bus controller **2772** is also coupled to expansion memory **2788** having RAM, ROM, and/or flash memory (not shown). The system **2700** may additionally include a memory module **2790** that is coupled to the bus controller **2712**. In one embodiment, the memory module **2790** comprises a ROM **2792** and flash (or EEPROM) **2794**.

[**0277**] As is familiar to those skilled in the art, the computer system **2700** further includes an operating system (OS) and at least one application program, which in one embodiment, are loaded into system memory **2724** from mass storage device **2752** and launched after POST. The OS may include any type of OS including, but not limited or restricted to, DOS, Windows™ (e.g., Windows 95™, Windows 98™, Windows NT™), Unix, Linux, OS/2, OS/9, Xenix, etc. The operating system is a set of one or more programs which control the computer system's operation and the allocation of resources. The application program is a set of one or more software programs that performs a task desired by the user.

[**0278**] In accordance with the practices of persons skilled in the art of computer programming, the present invention is described below with reference to symbolic representations of operations that are performed by computer system **2700**, unless indicated otherwise. Such operations are sometimes referred to as being computerexecuted. It will be appreciated that operations that are symbolically represented include the manipulation by CPU **2704** of electrical signals representing data bits and the maintenance of data bits at memory locations in system memory **2724**, as well as other processing of signals. The memory locations where data bits are maintained are physical locations that have particular electrical, magnetic, optical, or organic properties corresponding to the data bits.

[**0279**] When implemented in software, the elements of the present invention are essentially the code segments to perform the necessary tasks. The program or code segments can be stored in a processor readable medium or transmitted by a computer data signal embodied in a carrier wave over a transmission medium or communication link. The "processor readable medium" or "machine-readable medium" may include any medium that can store or transfer information. Examples of the processor readable medium include an electronic circuit, a semiconductor memory device, a ROM, a flash memory, an erasable ROM (EROM), a floppy diskette, a CD-ROM, an optical disk, a hard disk, a fiber optic medium, a radio frequency (RF) link, etc. The computer data signal may include any signal that can propagate over a transmission medium such as electronic network channels, optical fibers, air, electromagnetic, RF links, etc. The code segments may be downloaded via computer networks such as the Internet, Intranet, etc.

[**0280**] As discussed earlier, upon completion of the software and/or graphical user interface development process, the corresponding code may be stored in the database **24** or